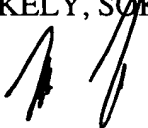


Remark

Applicants respectfully request reconsideration of this application as amended. Claims 1, 7, 13-16 have been amended. Claim 17 is new. Therefore, claims 1-17 are present for examination.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 1/9/03



Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980

Marked Version to Show Changes Made
Insertions are underlined and deletions bracketed.

1

- 1 1. (Amended) A method comprising:
- 2 receiving real-time analog data at a personal computer implementing a
- 3 general purpose operating system;
- 4 generating a real-time event at the personal computer indicating a request
- 5 to process the real time data;
- 6 determining whether the real-time event has a higher priority than a first
- 7 event being processed at the personal computer; and
- 8 [if so,] processing the real-time event if the real-time event has a higher
- 9 priority than the first event.

- 1 7. (Amended) A computer system comprising:
- 2 a chipset;
- 3 a bus coupled to the chipset; and
- 4 a central processing unit (CPU), [wherein the CPU] coupled to the bus,
- 5 that operates according to a general purpose operating system, [adaptable to
- 6 execute real-time instructions] and processes real-time data received at the
- 7 computer system.

13-
14-
1 (Amended) A central processing unit (CPU) comprising:
2 a timer to generate timing signals at predetermined time intervals;[and]
3 an event mechanism coupled to the timer to generate real time events in
4 response to receiving the timing signals and real-time data[, wherein the CPU
5 operates according to a general purpose operating system adaptable to execute
6 real-time instructions.]; and
7 an event handler coupled to the event mechanism to process the real-time
8 events received from the event mechanism,
9 the CPU operating according to a general purpose operating system.

1 14. (Amended) The computer system of claim 13 wherein the CPU further
2 comprises a register coupled to the event mechanism to store real-time data [an
3 event handler coupled to the event mechanism to process real-time events].

1 15. (Amended) The computer system of claim 14 wherein the [CPU further
2 comprises a register coupled to the event mechanism to store real-time data]
3 event handler verifies whether there is data stored in register upon detecting a
4 real-time event and determines the priority of the real-time event relative to
5 other interrupts received.

1 16. (Amended) The computer system of claim [15] 14 wherein the CPU
2 further comprises an analog to digital converter coupled to the register.

1 17. (New)